Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .0045” X .006”**

**Backside Potential: COLLECTOR**

**Mask Ref: DSA**

**APPROVED BY: DK DIE SIZE .024” X .026” DATE: 9/27/21**

**MFG: ALLEGRO / SPRAGUE THICKNESS .006” P/N: 2N3019**

**DG 10.1.2**

#### Rev B, 7/1